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**Date: 29-01-2021.**

**II.B.TECH- I-SEM (R22)-II MID Examinations-January-2024 Date: 22/01/2024**

**Subject: ADE Time*:* 01:30 TO 03:30 PM**

**Branch: IT & CSM Marks: 30 M**

***Answer all Questions in Part -A & Answer any FOUR Questions in Part -B***

**PART-A 5x2=10 M**

**BTL CO**

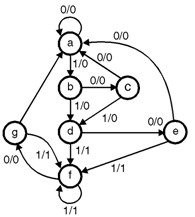
1. Draw CMOS Inverter? 5 3
2. Compare Standard Forms and Canonical forms? 4 6
3. Difference between combinational and sequential circuits? 4 5
4. State De Morgan’s law? 4 3
5. Define Priority Encoder? 1 6

**PART-B 4X5=20 M**

**BTL CO**

1. Obtain reduce state table and reduce state diagram for the sequential machine 3 5

whose state diagram is shown in the figure.



7. Explain the 32:1 Multiplexer using 16:1 Multiplexer 3 4

8 Minimize the following expressions using K-map and realize using NAND Gates. 3 4

F(A,B,C,D) = ∑m (0,2,3,6,7,8,10,12,13).

9. Explain the Modified DTL gate? 4 6

10. Explain detail about various types of ROM ? 5 6

11. Define and design Universal Shift Registers? 6 6

SCHEME OF EVALUATION

PART-A

|  |  |  |  |
| --- | --- | --- | --- |
| S NO | THEORY | MARKS | TOTAL |
| 1 | Draw CMOS Inverter? | 2 | 2 |
| 2 | Compare Standard Forms and Canonical forms? | 2 | 2 |
| 3 | Difference between combinational and sequential circuits? | 2 | 2 |
| 4 | State De Morgan’s law? | 2 | 2 |
| 5 | Define Priority Encoder? | 2 | 2 |

PART-B

|  |  |  |  |
| --- | --- | --- | --- |
| S NO | THEORY | MARKS | TOTAL |
| 6 | Obtain reduce state table and reduce state diagram for the sequential machine whose state diagram is shown in the figure.  C:\Users\CP\Desktop\download.png  (or) | 5 | 5 |
| 7 | a) define Multiplexer?  b) Explain the 32:1 Multiplexer using 16:1 Multiplexer | 1  4 | 5 |
| 8 | a) Explain K-Map and NAND gate.  b) Minimize the following expressions using K-map and realize using NAND Gates.  F(A,B,C,D) = ∑m (0,2,3,6,7,8,10,12,13).    (or) | 2  3 | 5 |
| 9 | Explain the Modified DTL gate? | 5 | 5 |
| S NO | THEORY | MARKS | TOTAL |
| 10 | a) what is ROM?  b)Explain detail about various types of ROM ?  (or) | 1  4 | 5 |
| 11 | a) Define Universal Shift Registers?  b) design the Universal Shift Registers? | 2    3 | 5 |